REMARKS

I. Introduction

Claims 1, 3-10, 12-15, 17-21, 23-30, 32-34, 36-43, 45 and 46 are pending in the Application. Claims 1, 4, 6, 9, 12-15, 21, 24, 26, 29, 34, 37, 39, 42, 45 and 46 have been amended. Applicant respectfully requests reconsideration in view of the foregoing amendments and these remarks.

II. Allowable Subject Matter

Applicant notes with appreciation that claims 13, 33 and 46 were allowed.

III. Objections

Claims 12, 13, 26, 45 and 46 were objected to because of informalities. Applicant has amended the claims to correct the noted informalities rendering this objection moot. No new matter has been added.

IV. Rejection of claims 8, 28 and 41 under 35 USC 112, second paragraph

Claims 8, 28 and 41 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully traverses the rejection.

Claim 8 is directed to a voltage buffer wherein the first resistance value of the switch corresponds to a programmable gain step. The Examiner has indicated that the term "step" makes the claim unclear. Applicant respectfully disagrees.

Applicant believes that the language presented is sufficiently clear. Applicant's claim is in apparatus form and does not recite method steps. Applicant respectfully asserts that the use of the word "step" does not automatically infer a method claim. Here, the term "step" refers to the incremental gain (either positive or negative) that results from an incremental advance(or retreat) of the programmable resistance. Applicant respectfully asserts that the claim is definite, and requests withdrawal of the 35 USC 112 rejection.

Claim 28 is directed to a device where a first resistance value of the switch corresponds to a programmable gain step for the third circuit. For reasons that are similar to those discussed above with respect to claim 8, Applicant respectfully asserts that Claim 28 is also definite, and requests withdrawal of the 35 USC 112 rejection.

Claim 41 is directed to voltage buffer where a first resistance value of the switching means corresponds to a programmable gain step for a circuit comprising the programmable resistance. For reasons that are similar to those discussed above with respect to claim 8, Applicant respectfully asserts that Claim 28 is also definite, and requests withdrawal of the 35 USC 112 rejection.

V. Rejection of claims under 35 USC 102

Claims 1, 3-7, 9, 10, 14, 15, 17, 19, 21, 23-27, 29, 30, 34, 36-40, 42 and 43 were rejected under 35 USC 102 as being anticipated by Burger, Jr. et al. United States Patent Number 5, 412, 346 (hereinafter "Burger"). Applicant respectfully traverses the rejection.

Claim 1 as amended is directed to a programmable gain voltage buffer that includes a gain stage and a programmable resistance that is **coupled in series** and in communication with the gain stage. Applicant respectfully asserts that Burger does not teach or suggest such a configuration.

Burger shows an amplifier 120 that includes an input resistance 131 and a feedback resistance network (including resistance 151 and switches 450, 452, 454 and 456). The feedback resistance network is configured in parallel with the gain element (i.e., amplifier 120). Conversely, Applicant's claimed buffer includes a gain stage and programmable resistance that are **coupled in series**. Applicant respectfully asserts that Applicant's claimed structure is fundamentally different from that shown in Burger. Further, Applicant respectfully asserts that Burger could not be modified to include Applicant's claimed series coupling without destroying the intended use of the Burger system (i.e., placing the feedback resistance network in series would create a configuration where gain was no longer adjustable). Accordingly, Applicant

respectfully asserts that Burger fails to teach or suggest Applicant's claimed series configuration and respectfully requests withdrawal of the 35 USC 102 rejection.

Claim 3, 5-7, 9 and 10 depend from claim 1 and are allowable for at least the same reasons set forth above with respect to claim 1.

Claim 4 is directed to a programmable gain voltage buffer that includes a programmable resistance coupled in series and in communication with a gain stage. Claim 4 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 14 is directed to a method that includes providing an output signal from an output point coupled between a gain stage and a programmable resistance of a voltage buffer, wherein the gain stage and the programmable resistance are configured in series. Claim 14 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 17 and 19 depend from claim 14 and are allowable for at least the same reasons set forth above with respect to claim 14.

Claim 15 is directed to a method that includes providing an output signal from an output point coupled between a gain stage and a programmable resistance of a voltage buffer, wherein the gain stage and the programmable resistance are configured in series. Claim 15 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 21 is directed to a device that includes a programmable resistance coupled in series and in communication with a gain stage. Claim 21 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 23, 25-27, 29 and 30 depend from claim 21 and are allowable for at least the same reasons set forth above with respect to claim 21.

Claim 24 is directed to a device that includes a programmable resistance coupled in series and in communication with a gain stage. Claim 24 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 34 is directed to a programmable gain voltage buffer that includes means for providing a programmable resistance coupled in series and in communication with a gain stage. Claim 34 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 36, 38-40, 42 and 43 depend from claim 34 and is allowable for at least the same reasons set forth above with respect to claim 34.

Claim 37 is directed to a programmable gain voltage buffer that includes means for providing a programmable resistance coupled in series and in communication with a gain stage. Claim 37 is allowable for at least the same reasons set forth above with respect to claim 1.

VI. Rejection of claims under 35 USC 103(a)

Claims 18 and 20 were rejected under 35 USC 103(a) as being unpatentable over Burger. Applicant respectfully traverses the rejection.

Claims 18 and 20 depend from claim 14 and is allowable for at least the same reasons set forth above with respect to claim 14.

Claims 1, 3-7, 9, 12, 14, 15, 17-21, 23-27, 29, 32, 34, 36-42 and 45 were rejected under 35 USC 103(a) as being unpatentable over Lau et al. United States Patent No. 6, 462, 588 (hereinafter "Lau"). Applicant respectfully traverses the rejection.

Claim 1 as amended is directed to a programmable gain voltage buffer that includes a gain stage and a programmable resistance that is coupled in series and in communication with the gain stage. The programmable resistance includes a plurality of switches in parallel with a **reference resistive element**. Applicant respectfully asserts that Lau does not teach or suggest such a configuration.

As the Examiner has correctly noted, Lau shows an amplifier circuit (Fig. 4) that includes a plurality of switching pairs of transistors ((186, 188) and (190, 192)) in parallel with transistors 182 and 184. The Examiner has indicated that transistors 182 and 184 are Applicant's claimed reference resistive element. Applicant respectfully disagrees. While Applicant concedes that the transistors may have an associated resistance, they are not functionally equivalent to Applicant's claimed reference resistive element as suggested by the Examiner. As Applicant has indicated in Applicant's specification (see Page 6, paragraph 20), the combination of a reference resistive element and transistor switches in parallel provides accurate programmability. As is suggested in the specification, the reference resistive element is the basis for such accuracy. The structure

of Lau does not provide the same advantages. The substitution of a switch for Applicant's reference resistive element will not produce a similarly accurate structure. Accordingly, Applicant respectfully asserts that Applicant's claimed structure is not equivalent to that shown in Lau. Accordingly, Applicant respectfully asserts that Lau fails to teach or suggest Applicant's claimed reference resistive element and respectfully requests withdrawal of the 35 USC 103 rejection.

Claims 3, 5-7, 9 and 12 depends from claim 1 and is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 4 is directed to a programmable gain voltage buffer that includes a programmable resistance that includes a reference resistive element. Claim 4 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 14 is directed to a method that includes activating one or more selected switches in a plurality of switches in parallel with a predominant reference resistive element in the voltage buffer. Claim 14 is allowable for at least the same reasons set forth above with respect to claim 1. In addition, Claim 14 is separately allowable for at least the additional reason that Claim 14 sets forth a method that recites that the reference resistive element be **predominant**. Lau does not teach or suggest any relationship to the relative sizes or impact on the programmability of its transistors 182 and 184 to the structure. Accordingly, Applicant respectfully asserts that Applicant's claimed predominant reference resistive element is not taught or suggested by Lau.

Claims 17-20 depend from claim 14 and are allowable for at least the same reasons set forth above with respect to claim 14.

Claim 15 is directed to a method that includes activating one or more selected switches in parallel with a predominant reference resistive element in the voltage buffer. Claim 15 is allowable for at least the same reasons set forth above with respect to claim 1. In addition, Claim 15 is separately allowable for at least the additional reason that Claim 15 sets forth a method that recites that the reference resistive element be predominant. As discussed above with respect to Claim 14, Lau does not teach or suggest any relationship to the relative sizes or impact on the programmability of its transistors 182 and 184 to the structure. Accordingly, Applicant

respectfully asserts that Applicant's claimed predominant reference resistive element is not taught or suggested by Lau.

Claim 21 is directed to a device that includes a programmable resistance that includes a reference resistive element. Claim 21 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 23, 25-27, 29 and 32 depend from claim 21 and are allowable for at least the same reasons set forth above with respect to claim 21.

Claim 24 is directed to a device that includes a programmable resistance that includes a reference resistive element. Claim 24 is allowable for at least the same reasons set forth above with respect to claim 1.

Claim 34 is directed to a programmable gain voltage buffer that includes means for providing a programmable resistance including a reference resistive means. Claim 34 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 36, 38-42 and 45 depend from claim 34 and are allowable for at least the same reasons set forth above with respect to claim 34.

Claim 37 is directed to a programmable gain voltage buffer that includes means for providing a programmable resistance including reference resistive means. Claim 37 is allowable for at least the same reasons set forth above with respect to claim 1.

Pursuant to 37 CFR §1.136, Applicant hereby petitions that the period for response to the office action dated January 18, 2006, be extended for three months to and including July 18, 2006.

A submission of Credit Card Payment Request authorizing the above fee of $1020 is enclosed.

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Page : 19 of 19

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Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date: 7/18/06

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